FPD-link, 30-Bits Color LVDS Receiver, 170Mhz (SVGA/Full-HD)
LVDS de-serializer 5:35 channel decompression with automatic de-skew
40nm Logic Salicide 1.1V/2.5V

Overview:

V-Trans 's FPD Link Receiver Macro is based on National Semiconductor openLDI specification v0.95 dated May 13th 1999 that allow the transfer of digital display data between a display source and a display device.

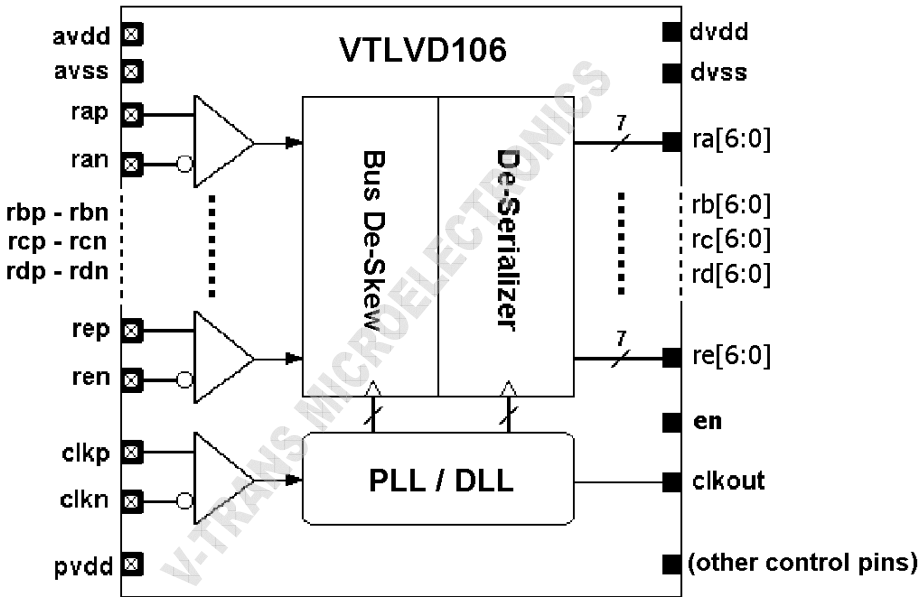
This receiver converts 5 LVDS, (low voltage differential signaling) data streams, into 30bits (single pixel) CMOS data plus 5 control signals (VSYNC, HSYNC, DE, and 2 user-defined signals).

Thanks to its innovative lane to lane de-skew mechanism this macro can operate up to a maximum pixel rate of 170Mhz, LVDS data line speed is 1.19Gb/s, providing a total maximum bandwidth of 5.95Gb/s (744Mbytes per second).

Features:

- 1P7M/1P8M/1P9M/1P10M layout structure based on 40nm Logic 1P10M Salicide 1.1V/2.5V process.
- 1.1V/2.5V ±10% supply voltage, -40/+125°C
- Complies with OpenLDI specification for digital display interfaces and LVDS IEEE Standard 1596.3-1996+ ANSI/TIA/EIA-644-A Specifications.
- Up to 5.6Gbps bandwidth (40 to 170Mhz pixel clock) (supports Full HDTV 1080p)
- +/-0.3 UI bus de-skew, relaxes timing constraint
- Input clock detector (self reset when missing clock)
- Spread-spectrum input clock support (can be used in SS systems)
- Core cell area : [contact us]
- Power consumption [contact us] @150Mhz
- Built-in power pads with ESD protection.
- Low leakage power-down mode <1uA.

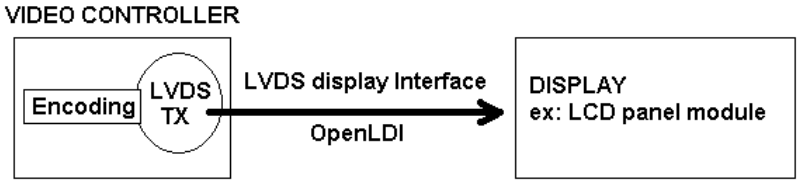
Block Diagram:



Application:

This interface is suitable for TCON chips inside Flat panel displays, as a FPD-Link receiver.

Flat panel displays application:



Common resolution:

Resolution	Vertical Frame Rate (Hz)	Pixel Rate (MHz)
SVGA 800 x 600	60	40
	75	49.5
	85	56.25
XGA 1026 x 768	60	65
	75	78.75
	85	94.5
WXGA / HDTV 1280 x 720p	60	74.25
	120	148.5
WXGA 1366 x 768	60	82
	75	122
SXGA 1280 x 1026	60	108
	75	135
	85	157.5
SXGA+ 1400 x 1050	60	124
UXGA 1600 x 1200	60	162
	65	175
	70	189
UXGAW 1900 x 1200	60	180
Full HDTV 1920 x 1080p	60	148.5
	120	297
	240	594
Cinema Full HD 2560 x 1080p	60	185
	120	370
4k x 2k 3840 x 2160p	60	594
	120	1188

Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement.
In most cases, the physical is merged on foundry site.

Design Kit

Design kit includes :

- LEF view and abstract gdsII
- Verilog HDL behavioral model
- Liberty (.lib) timing constraints for typical, worse and best corner case
- Full Datasheet /Application Note with integration guidelines document
- Silicon characterization report when available

Tapeout Kit

Tapeout kit includes the design kit plus plysical view:

- gdsII
- LVS netlist and report
- DRC/ERC/ESD/ANT report

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs .

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule.
Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS serdes, Display Interfaces, DDRII, DDR3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL.)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset..)
- Video and WIMAX Analog Front end

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