Triple 10-Bits Video DAC, 240Mhz

Overview:

This IP is composed of a triple channel 10-bits 240 MS/s DAC, designed for industry standard 0.18um 1P6M CMOS technology supplied at 3.3V.

Each independent DAC uses a segmented current steering architecture, combined with improved two-dimensional centroid switching scheme, to achieve simultaneously high update rates, at least 10-bit of intrinsic static accuracy, and a very good dynamic characteristics.

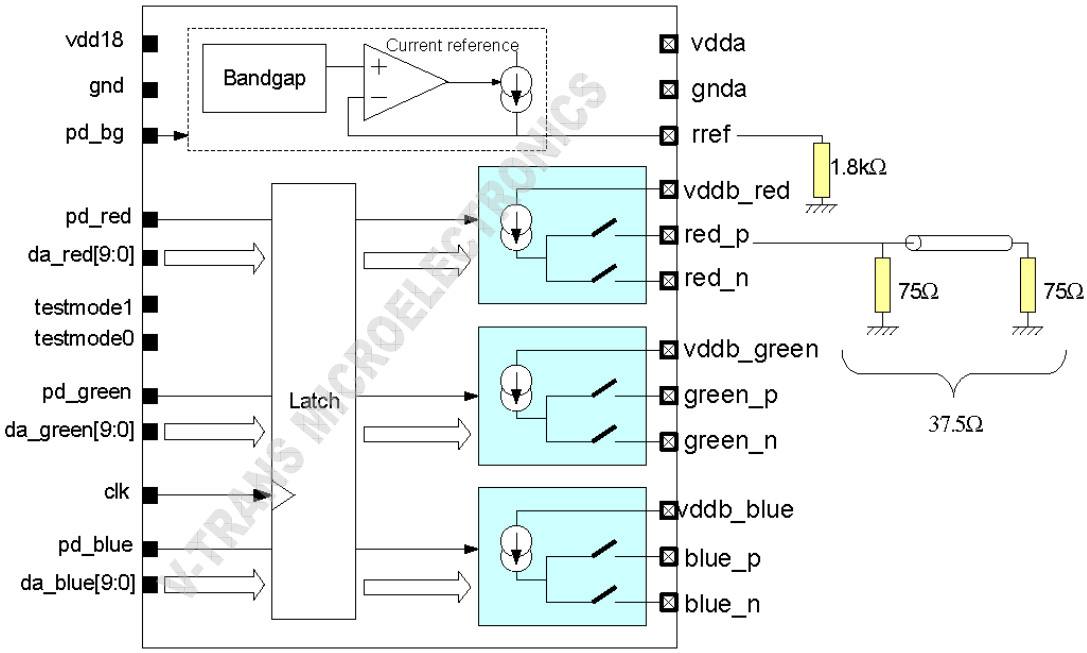
The differential output supports single-ended applications and is designed to be loaded by double 75Ω line termination, (37.5Ω).

An external resistor, 1k8Ω typical is used to set the full scale current of the DAC.

Features:

- 10-Bits Resolution
- 240MS/s Update Rate
- 3.3V ±10% supply voltage, -40/+125°C temperature.
- 1P6M layout structure based on 0.18um 1P6M 3.3V/1.8V generic logic process.
- Individual DAC channel Power down.
- Do not require extra external bias circuit.
- Cell area: [contact us)
- Built in I/Os with ESD protection on 75um pad pitch.
- Antenna diodes on each digital input.
- Silicon proven.

Block Diagram:



10 Bits Video DAC

Application: Video signal generation.

Electrical Specification:

General :

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*
Tj	Junction Temperature	0	70	125	ºC
vdda	Analog power supply	3.0	3.3	3.6	V
vddb_*	Channel power supply	3.0	3.3	3.6	V
vdd18	Core power supply	1.62	1.8	1.98	V

Symbol	*Parameter*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Res	Resolution			10		Bits
Freq	Max frequency update				240	Mhz
Rref	Reference resistor value			1k8		Ω
Voutpp	Differential peak to peak output	(red_p-red_n)		2.6		Vpp
Vout	Single-ended output	red_p		1.3		V
Vcm	Output common mode level	Rref=1.8kΩ		0.65		V
Code	Input code			binary		
INL				± 1	± 2	LSB
DNL				± 0.5	± 1	LSB
SNR				61		dB
SFDR		1Mhz, -1 dBFS sine input	-55			dB
THD				-73		dB
PSSR	Power supply rejection					dB
Pdiss	Power dissipation	FF corner, 0degC, 3.6V/1.98V @100Mhz	-	-	ontact u	mA
Td	Analog output delay	from CLK=Vih(min) to 50% of full scale transistion				ns
Thold	Input data hold time					ps
Tsetup	Input data setup time					ps

ESD immunity

+/-2KV HBM based on Mil Std. 883 Method 3015.7
+/-500V CDM,
+/-200V MM

Latch-up immunity

minimum +/-300mA injection at 100C based on EIA/JESD78

Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement.
In most cases, the physical is merged on foundry site.

Design Kit

Design kit includes :

- LEF view and abstract gdsII
- Verilog HDL behavioral model
- Liberty (.lib) timing constraints for typical, worse and best corner case
- Full Datasheet /Application Note with integration guidelines document
- Silicon characterization report when available

Tapeout Kit

Tapeout kit includes the design kit plus plysical view:

- gdsII
- LVS netlist and report
- DRC/ERC/ESD/ANT report

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs using cheaper technologies such as 0.18um.

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule.
Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS serdes, Display Interfaces, DDRII, DDR3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL.)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset..)
- Video and WIMAX Analog Front end

V-TRANS Microelectronics – Shanghai Office
Tel: (+86)-021-54234123
v-trans@v-trans.com