

**Dual RSDS Transmitter, 24-bit color, 40-300Mb/s (SVGA/UXGA/Full HDTV)
0.18um 1P6M Generic Logic Process****Overview:**

This RSDS Transmitter interface IP is based on RSDS “Intra-Panel” Interface Specification rev1.0, dated May 2003 that allow the transfer of digital display data between a Timing Control source (TCON) and Column Drivers of a Flat Panel Display.

The transmitter converts up to 24-bit DDR CMOS data (single pixel 18-bit, single pixel 24-bit, dual pixel 18-bit, dual pixel 24-bit color) into 24 RSDS, (Reduced Swing Differential Signaling) data streams.

At a maximum dual pixel rate of 150Mhz, RSDS data line speed is 300Mbps, providing a total throughput of 7.2Gbps (900MegaBytes per second).

All the data input/output are independent from each other and can be assigned following any partitioning to support all LCD and Plasma display panel system architectures. (RGB, front/back, even/odd, mixed RGB etc...)

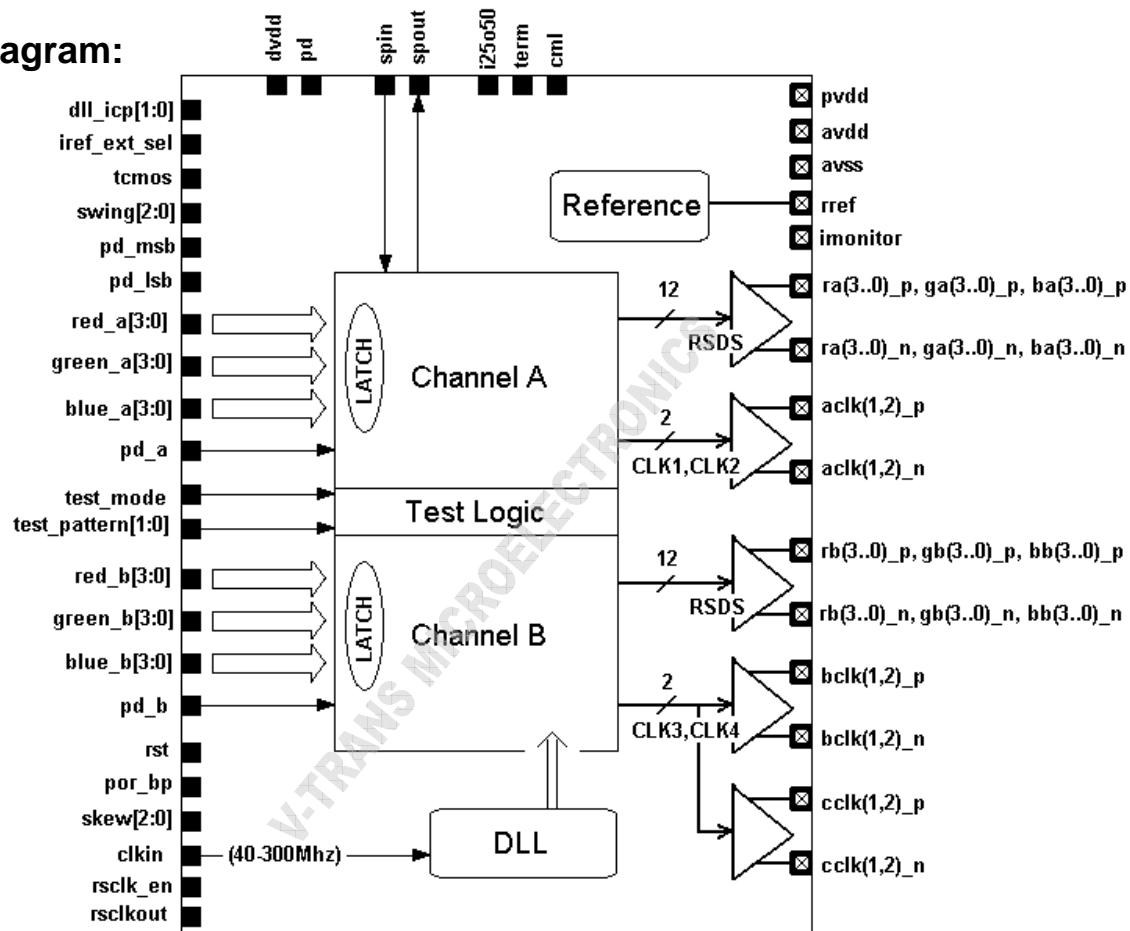
Each pixel channel has 2 identical clock outputs. Strength of the RSDS I/Os can be adjusted from 2mA nominal to 4mA in order to support both 100Ω and 50Ω termination.

For convenient routing when TCON is mounted on top or bottom of a display panel, a selectable output data mapping is usually available. LSB or MSB of both channels can be forced to High-Z in order to support 18-bit data color.

This IP can interface with both 1.8V or 3.3V core logic, giving more flexibility for the design.

Features:

- 20 to 150Mhz Pixel rate (40 to 300 Mb/s SDR input, 40 to 300 Mb/s DDR output)
- Complies with RSDS “Intra-Panel” Interface Specification rev1.0, May 2003.
- 1P6M layout structure based on 0.18um 1P6M generic logic process.
- $3.3V/1.8V \pm 10\%$ supply voltage, $-40/+125^\circ C$
- For either 3.3V only or 1.8V/3.3V design.
- Dual pixel architecture up to 7.2Gbps bandwidth
- 6x RSDS clock channels
- Low EMI
- 24 and 18 Bits color & reverse output mapping support
- Self Power-On-Reset feature
- Precise RSDS clock skew adjustment using DLL
- Phase-shifted clock output to core to support additional CD control signals
- Accurate output current digital control
- Built-in power pads with ESD protection
- Low leakage power-down mode $< 2\mu A$.
- Low power consumption, [contact us]
- Very compact cell area : [contact us]

Block Diagram:**Application:**

This interface is to be used by Timing Controller (TCON) ASICs to drive Column Drivers of LCD or Plasma Display Panel.

Common resolution:

Resolution	Vertical Frame Rate (Hz)	Pixel Rate (MHz)
SVGA 800 x 600	60	40
	75	49.5
	85	56.25
XGA 1024 x 768	60	65
	75	78.75
	85	94.5
SXGA 1280 x 1024	60	108
	75	135
	85	157.5
UXGA 1600 x 900	60	162
	65	175
	70	189
Full HDTV 1920 x 1080	60	165

Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement.
In most cases, the physical is merged on foundry site.

Design Kit

Design kit includes :

- LEF view and abstract gdsII
- Verilog HDL behavioral model
- Liberty (.lib) timing constraints for typical, worse and best corner case
- Full Datasheet /Application Note including integration guidelines
- Silicon characterization report when available

Tapeout Kit

Tapeout kit includes the design kit plus physical view:

- gdsII
- LVS netlist and report
- DRC/ERC/ESD/ANT report

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs using cheaper technologies such as 0.18um.

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule.
Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS SerDes, Display Interfaces, DDR2/3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL.)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset..)
- Video Analog Front end

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Rev 2.4