LVDS Receiver 1250Mb/s, 800Mhz clock, (staggered)

Overview:

V-Trans 's LVDS technology solutions eliminate the trade-offs in speed, low power, low noise (EMI), and BOM cost saving for high performance data transmission applications.

This LVDS receiver is a very fast comparator that can recover very small differential signaling with a very wide common mode range, allowing a proper recovery of LVDS signals and its use with many other specification.

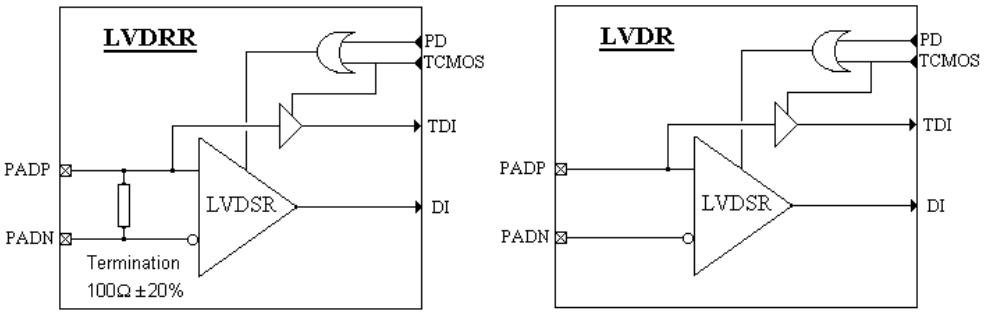
Two separate library are available: inline (VT18LVDSR-I) and staggered I/O configuration (VT18LVDSR-S).

This library use Staggered I/O pitch of 40um, for high integration of wide LVDS buses.

Features:

- 1P6M layout structure based on 0.18um 1P6M 1.8V generic logic process.
- 3.3V/1.8V ±10% supply voltage, -40/+125°C temperature.
- IEEE Standard 1596.3-1996 and ANSI/TIA/EIA-644-A Specifications.
- Up to 1250Mb/s DDR, or 800Mhz clock.
- Optional 100Ω on die termination.
- Power down mode.
- CMOS input for chip testability (JTAG…)
- Rail to Rail Input common mode for extended compatibility with other specification.
- Do not require extra external bias circuit.
- Staggered compact design x=80um y=300um
- Small area : 0.024 mm2
- Comes with a set of ESD protected power pads, corner, filler and break cells for easy integration.
- Silicon proven, and test report available.

Block Diagram:



Application:

The high-speed, low power, low noise/EMI and low cost benefits of LVDS broaden the scope of LVDS applications far beyond those for traditional technologies. Here are some examples:

- Flat panel displays,
- Set top boxes
- Printers
- In flight/car entertainment
- 3G base station (clock tree)
- Cell phones, PDA
- Military communications
- Clock buffer/distribution
- High speed comparator
- ADC / DAC low noise digital interface

Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement.
In most cases, the physical is merged on foundry site.

Design Kit

Design kit includes :

- LEF view and abstract gdsII
- Verilog HDL behavioral model
- Liberty (.lib) timing constraints for typical, worse and best corner case
- Full Datasheet /Application Note with integration guidelines document
- Silicon characterization report when available

Tapeout Kit

Tapeout kit includes the design kit plus plysical view:

- gdsII
- LVS netlist and report
- DRC/ERC/ESD/ANT report

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs using cheaper technologies such as 0.18um.

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule.
Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS serdes, Display Interfaces, DDRII, DDR3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL.)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset..)
- Video and WIMAX Analog Front end

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