FPD-link Transmitter, 24 Bits Color, 20-135 Mhz (SVGA/SXGA)
LVDS serializer 28:4 channel compression

Overview:

This FPD Link Transmitter Macro is based on National Semiconductor openLDI specification v0.95 dated May 13th 1999 that allow the transfer of digital display data between a display source and a display device.

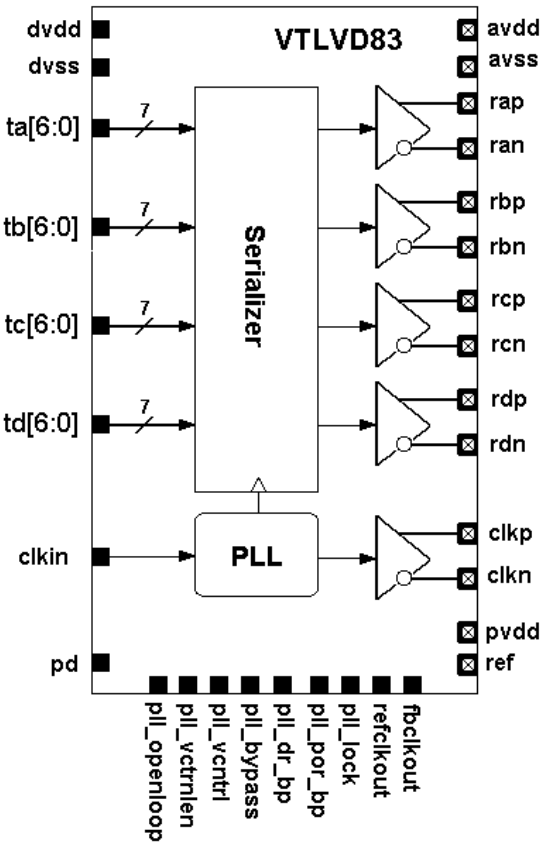
This transmitter converts 4 LVDS, (low voltage differential signaling) data streams, into up to 24 bits CMOS data plus 4 control signals (VSYNC, HSYNC, DE, and 1 user-defined signals).

At a maximum pixel rate of 135Mhz, LVDS data line speed is 945Mbps, providing a total maximum bandwidth of 3.78Gb/s (472Mbytes per second).

Features:

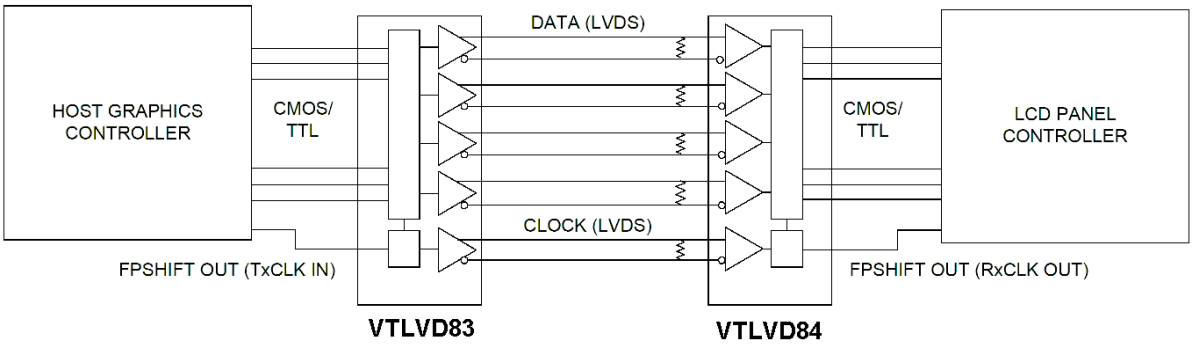
- 1P6M layout structure based on 0.13um 1P6M 1.8V/3.3V generic logic process.
- 3.3V/1.8V ±10% supply voltage, 0/+125°C
- Complies with OpenLDI specification for digital display interfaces and LVDS IEEE Standard 1596.3-1996+ ANSI/TIA/EIA-644-A Specifications.
- Up to 3.78Gbps bandwidth (135Mhz pixel clock)
- Spread-spectrum input clock support (can be used in SS systems)
- Output Swing Control (2.5mA to 7mA), PVT compensated
- Core cell area: [contact us]
- Built-in power pads with ESD protection.
- Low leakage power-down mode <10uA.
- Equivalent part : Thine's THC63LVD83

Block Diagram:



Application:

This interface is suitable to drive a TCON chips inside Flat panel displays, as a FPD-Link transmitter.
It can also be used as 28:4 LVDS compression channel (serializer).



Common resolution:

Resolution	Vertical Frame Rate (Hz)	Pixel Rate (MHz)
SVGA 800 x 600	60	40
	75	49.5
	85	56.25
XGA 1024 x 768	60	65
	75	78.75
	85	94.5
WXGA / HDTV 1280 x 720	60	56
	75	70
WXGA 1366 x 768	60	82
	75	122
SXGA 1280 x 1024	60	108
	75	135
	85	157.5
UXGA 1600 x 1200	60	162
	65	175
	70	189
Full HDTV 1920 x 1080	60	165

Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement.
In most cases, the physical is merged on foundry site.

Design Kit

Design kit includes :

- LEF view and abstract gdsII
- Verilog HDL behavioral model
- Liberty (.lib) timing constraints for typical, worse and best corner case
- Full Datasheet /Application Note with integration guidelines document
- Silicon characterization report when available

Tapeout Kit

Tapeout kit includes the design kit plus plysical view:

- gdsII
- LVS netlist and report
- DRC/ERC/ESD/ANT report

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs using cheaper technologies such as 0.18um.

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule.
Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS serdes, Display Interfaces, DDRII, DDR3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL.)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset..)
- Video and WIMAX Analog Front end

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