10-Bits ADC, 110Mhz - 3.3V

Overview:

This Analog -to-Digital converter IP has a monolithic differential pipelined architecture with output error correction logic providing 10 bits conversion accuracy from 10 up to 110 Mhz sampling frequency.
It is designed for industry standard 0.18um 1P6M CMOS technology supplied at 3.3V.

This ADC can interface with both 1.8V or 3.3V core logic, by connecting dvdd to 1.8V or 3.3V power line, giving more flexibility for design reuse.

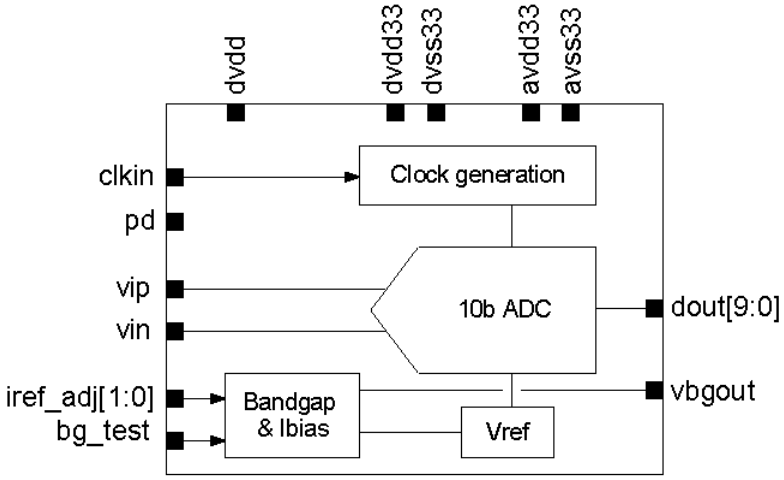
Features:

- 10-Bits pipeline architecture
- 110MS/s sampling rate
- 1.5Vp-p differential input
- 3.3V ±10% supply voltage, -40/+125°C temperature.
- 1P6M layout structure based on 0.18um 1P6M 3.3V/1.8V generic logic process.
- Fully differential architecture
- Area: [contact us]
- Power consumption

[contact us]

- Power down leakage current <1uA
- Antenna diodes on each digital input.
- uses MIM capacitor

Block Diagram:



Application:

- Communication Receiver Channel
- Mobile TV
- Digital Imaging/video
- Graphic capture

Electrical Specification:

General :

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*
Tj	Junction Temperature	0	70	125	ºC
avdd33	Analog power supply	3.0	3.3	3.6	V
dvdd33	Digital power supply	3.0	3.3	3.6	V
dvdd	Core power supply (*)		1.8/3.3		V

(*) dvdd can be either connected to 1.8V or 3.3V in order to accommodate both core logic.

Symbol	*Parameter*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Res	Resolution			10		Bits
Fs	Sampling frequency		10		110	Mhz
Vin-pp	Differential full-scale input	|Vip-Vin|			1.5	Vpp
Bwth	Analog Input bandwidth	-3dB	300			Mhz
Zin	Input impedance	switched cap		0.6		pF
∆Vref	Internal differential reference voltage			0.75		V
Code	Output code	offset binary		binary		
INL	Integral non-linearity			± 1	± 2	LSB
DNL	Differential non-linearity			± 0.5	± 1	LSB
SNR	Signal to noise ratio		52			dBFS
SNDR	Signal to noise and distorsion ratio		52			dBFS
SFDR	Spurious free dynamic range		60			dBc
ENOB	Equivalent number of bits	FS=110Mhz, Fin=10Mhz	8	8.5	9	Bits
I(dvdd33)	Digital current consumption	Fs=110Mhz	-			mA
I(avdd33)	Analog current consumption	Fs=110Mhz	-			mA
Ileak	Leakage current	powerdown mode			1	uA
Latency	Pipeline latency			8		clocks
twakeup	Powerdown to active state time					us
Area	Layout area					mm2

Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement.
In most cases, the physical is merged on foundry site.

Design Kit

Design kit includes :

- LEF view and abstract gdsII
- Verilog HDL behavioral model
- Liberty (.lib) timing constraints for typical, worse and best corner case
- Full Datasheet /Application Note with integration guidelines document
- Silicon characterization report when available

Tapeout Kit

Tapeout kit includes the design kit plus plysical view:

- gdsII
- LVS netlist and report
- DRC/ERC/ESD/ANT report

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs using cheaper technologies such as 0.18um.

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule.
Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS serdes, Display Interfaces, DDRII, DDR3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL.)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset..)
- Video and WIMAX Analog Front end

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