Dual RSDS Transmitter, 30-bit color, 80-400Mb/s (SVGA/Full HDTV@120Hz)

0.13um Logic Process

Overview:

This RSDS Transmitter interface IP is based on RSDS "Intra-Panel" Interface Specification rev1.0, dated May 2003 that allow the transfer of digital display data between a Timing Control source (TCON) and Column Drivers of a Flat Panel Display.

The transmitter converts up to 30-bit DDR CMOS data (single pixel 24-bit, single pixel 30-bit, dual pixel 24-bit, dual pixel 30-bit color) into 30 RSDS, (Reduced Swing Differential Signaling) data streams.

At a maximum Dual pixel rate of 200Mhz (x2), RSDS data line speed is 400Mbps/lane, providing a total throughput of 12Gbps (1.5GygaBytes per second).

All the data input/output are independent from each other and can be assigned following any partitioning to support all LCD and Plasma display panel system architectures. (RGB, front/back, even/odd, mixed RGB etc…)

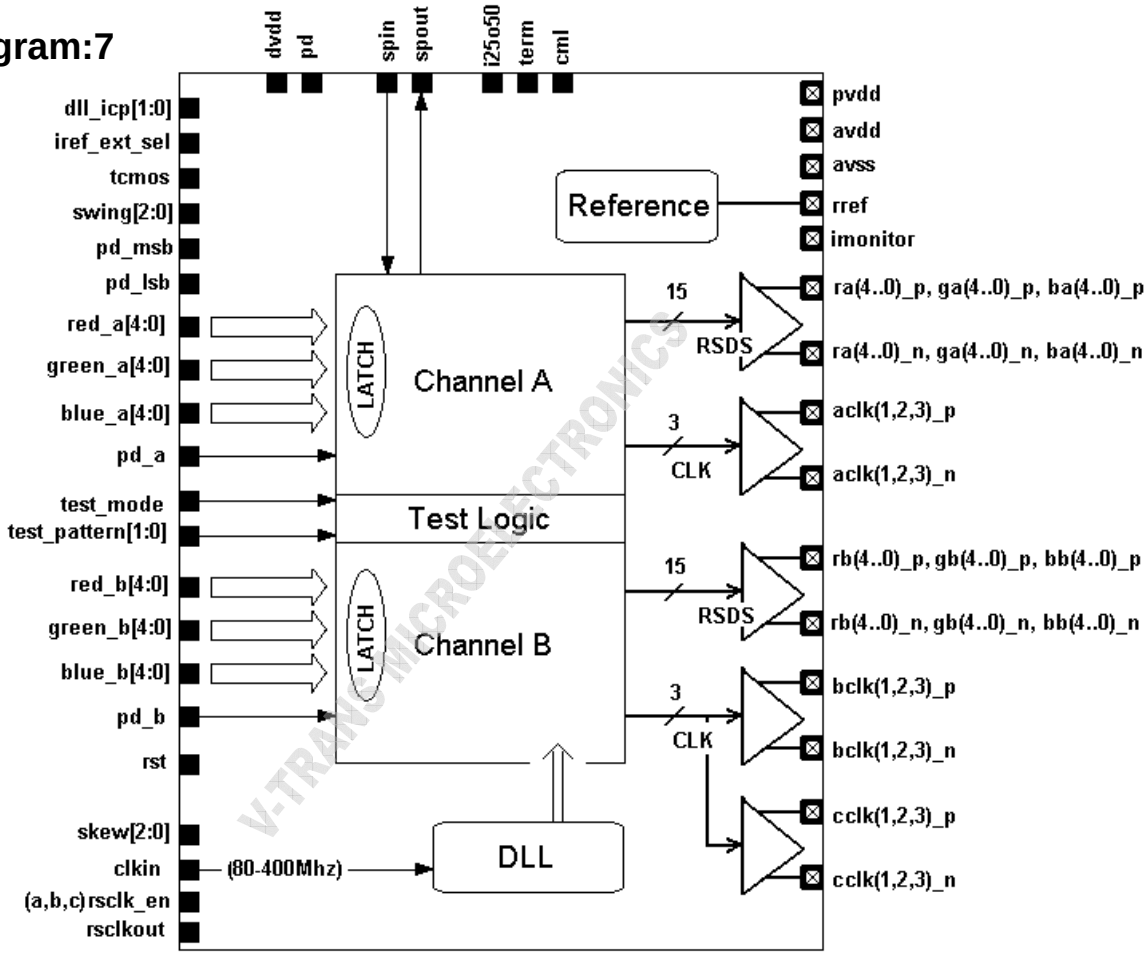
Each pixel channel has 3 identical clock outputs. Strength of the RSDS I/Os can be adjusted from 2mA nominal to 4mA in order to support both 100Ω and 50Ω termination. Tree (3) extra clock outputs are also provided.

For convenient routing when TCON is mounted on top or bottom of a display panel, a selectable output data mapping is usually available. LSB or MSB of both channels can be forced to High-Z in order to support 24-bit data color.

Features:

- 40 to 200 Mhz Pixel rate per channel (80 to 400 Mb/s SDR input, 80 to 400 Mb/s DDR output)
- Complies with RSDS "Intra-Panel" Interface Specification rev1.0, May 2003.
- 1P6M, 1P7M or 1P8M layout structure based on 0.13um 1P8M logic process.
- 3.3V/1.2V ±10% supply voltage, -40/+125°C
- Dual pixel architecture up to 12Gbps bandwidth
- 9x RSDS clock channels
- Output signal strength is highly adjustable and is PVT compensated
- Low EMI
- 30 and 24 Bits color & reverse output mapping support
- Self Power-On-Reset feature
- Precise RSDS clock skew adjustment using DLL
- Phase-shifted clock output to core to support additional CD control signals
- Built-in power pads with ESD protection
- Low power consumption, [contact us] @330Mb/s (HDTV@120Hz)
- Low leakage power-down mode < 2.8uA
- Compact cell area : [contact us]
- Innovative approach allows lower bounding pad count

Block Diagram:7



Application:

This interface is to be used by Timing Controller (TCON) ASICs to drive Column Drivers of LCD or Plasma Display Panel.

Common resolution:

Resolution	Vertical Frame Rate (Hz)	Pixel Rate (MHz)
SVGA 800 x 600	60	40
	75	49.5
XGA 1024 x 768	60	65
	75	78.75
SXGA 1280 x 1024	60	108
	75	135
	85	157.5
UXGA 1600 x 900	60	162
	65	175
	70	189
Full HDTV 1920 x 1080	60	165
	120	330
	240	660

Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement.
In most cases, the physical is merged on foundry site.

Design Kit

Design kit includes :

- LEF view and abstract gdsII
- Verilog HDL behavioral model
- Liberty (.lib) timing constraints for typical, worse and best corner case
- Full Datasheet /Application Note including integration guidelines
- Silicon characterization report when available

Tapeout Kit

Tapeout kit includes the design kit plus plysical view:

- gdsII
- LVS netlist and report
- DRC/ERC/ESD/ANT report

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs .

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule.
Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS serdes, Display Interfaces, DDRII, DDR3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL.)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset..)
- Video Analog Front end

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