

Dual FPD-link Transmitter, 30/24-bits color, 40-170 Mhz (SVGA/UXGA) LVDS serializer 70:10 channel compression – Full HDTV @120Hz

Overview:

This FPD-Link Transmitter Macro is based on National Semiconductor openLDI specification v0.95 dated May 13th 1999 that allow the transfer of digital display data between a display source and a display device.

This transmitter converts 10 LVDS, (low voltage differential signaling) data streams, into up to 60 bits (dual pixel 30-bits) CMOS data plus 10 control signals (VSYNC, HSYNC, DE, and 7 user-defined signals).

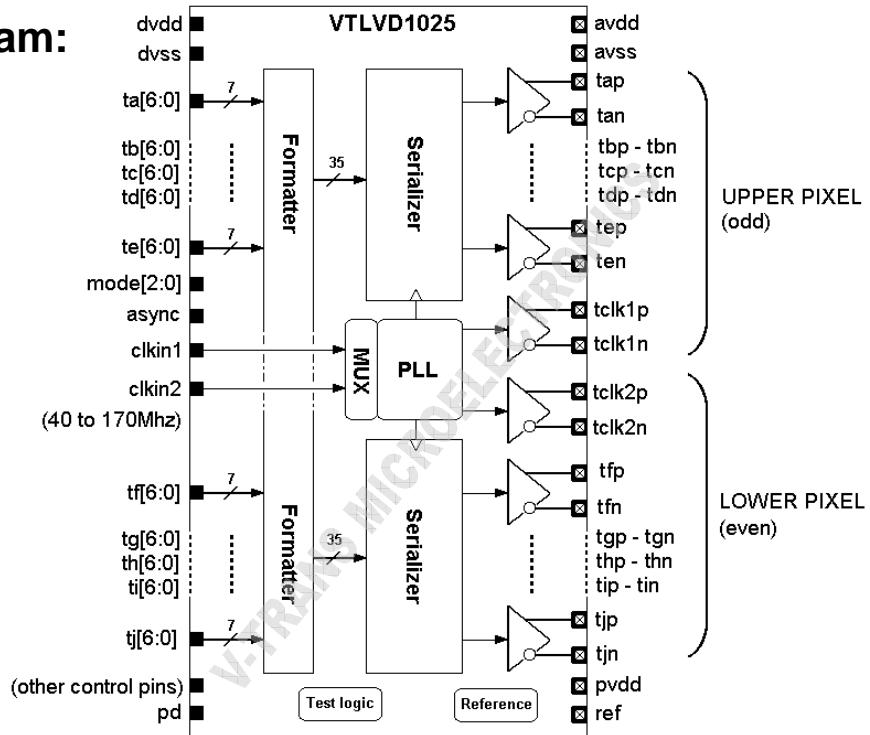
At a maximum pixel rate of 170Mhz, LVDS data line speed is 1.19Gbps, providing a total maximum bandwidth of 11.9Gb/s (1.487Gbytes per second).

This IP can drive two (2) independent displays with resolution up to UXGA/Full HD (dual asynchronous input /output).

Features:

- 1P6M/1P7M/1P8M layout structure based on 0.13um Logic 1P8M Salicide 1.2V/3.3V process.
- 1.2V/3.3V $\pm 10\%$ supply voltage, -40/+125°C
- Complies with OpenLDI specification for digital display interfaces and LVDS IEEE Standard 1596.3-1996+ ANSI/TIA/EIA-644-A Specifications.
- Up to 11.9Gbps bandwidth (40 to 170Mhz pixel clock) per pixel channel (Full HD @ 120Hz)
- Dual independent single link mode (can drive 2 separate displays with different resolution)
- Input clock detector (self reset when missing clock)
- Spread-spectrum input clock support (can be used in SS systems)
- Output Swing Control (2.5mA to 7mA programmable), PVT compensated
- Input clock detector (self reset when missing clock)
- Low leakage power-down mode <10uA
- Core cell area : [contact us]
- Power consumption [contact us]
- Built-in power pads with ESD protection.
- Equivalent part : Thine's THC63LVD1025

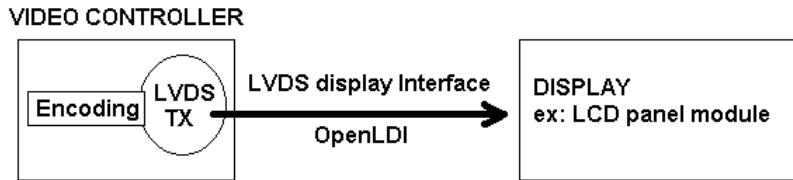
Block Diagram:



Application:

This interface is suitable to drive a TCON chips inside Flat panel displays, as a FPD-Link transmitter.

Flat panel displays application:



Common resolution:

Resolution	Vertical Frame Rate (Hz)	Pixel Rate (MHz)
SVGA 800 x 600	60	40
	75	49.5
	85	56.25
XGA 1024 x 768	60	65
	75	78.75
	85	94.5
WXGA / HDTV 1280 x 720p	60	74.25
	120	148.5
WXGA 1366 x 768	60	82
	75	122
SXGA 1280 x 1024	60	108
	75	135
	85	157.5
SXGA+ 1400 x 1050	60	124
UXGA 1600 x 1200	60	162
	65	175
	70	189
UXGAW 1900 x 1200	60	180
Full HDTV 1920 x 1080p	60	148.5
	120	297
	240	594
Cinema Full HD 2560 x 1080p	60	185
	120	370
4k x 2k 3840 x 2160p	60	594
	120	1188

Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement.
In most cases, the physical is merged on foundry site.

Design Kit

Design kit includes :

- LEF view and abstract gdsII
- Verilog HDL behavioral model
- Liberty (.lib) timing constraints for typical, worse and best corner case
- Full Datasheet /Application Note with integration guidelines document
- Silicon characterization report when available

Tapeout Kit

Tapeout kit includes the design kit plus physical view:

- gdsII
- LVS netlist and report
- DRC/ERC/ESD/ANT report

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs .

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule.
Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS serdes, Display Interfaces, DDRII, DDR3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL.)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset..)
- Video and WIMAX Analog Front end

V-TRANS Microelectronics – Shanghai Office
Tel: (+86)-021-54234123
v-trans@v-trans.com