Low jitter, Audio Fractional-N PLL

Overview:

This PLL can generate all the frequencies used by audio systems from any stable clock between 10 and 40Mhz.

Audio clock is $256 \times f_s0$ or $384 \times f_s1$, where $f_s0$ is 192kHz or 176.4kHz and $f_s1$ is 96kHz or 88.2Khz. An output divider by $N$ generates multiple of 192kHz, 176.4kHz, 96kHz, 88.2kHz, 48kHz, 44.1kHz, 32kHz, 24kHz, 22.050kHz, 16kHz, 12kHz, 11.025kHz, and 8kHz frequencies.

An external reference current is required, and can be provided either by V-Trans Irefgen (resistor-less design +/-5%) or Refgen (with external reference resistor +/-1%) libraries or any other third party IP.

Features:

- Fractional-N PLL : ± 0.05 ppm accuracy
- Eliminates VCXO/DCXO requirements
- 10-40 Mhz input
- Audio clock supports $256 \times f_s$ & $384 \times f_s$
- 3.3V/1.8V ±10% supply voltage, -40/+125°C
- 1P6M layout structure based on 0.18um 1P6M 3.3V/1.8V generic logic process.
- Small cell area with integrated loop filter: [contact us]
- Low jitter : [contact us]
- 50% duty cycle output.
- Antenna diodes on each digital input.
- Silicon proven.

Block Diagram:

Application:

- Audio systems
- Clock synthesis for audio DAC
Deliverables:

V-Trans provides 2 separate kits depending on licensing agreement. In most cases, the physical is merged on foundry site.

<table>
<thead>
<tr>
<th>Design Kit</th>
<th>Tapeout Kit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design kit includes :</td>
<td>Tapeout kit includes the design kit plus physical view:</td>
</tr>
<tr>
<td>- LEF view and abstract gdsII</td>
<td>- gdsII</td>
</tr>
<tr>
<td>- Verilog HDL behavioral model</td>
<td>- LVS netlist and report</td>
</tr>
<tr>
<td>- Liberty (.lib) timing constraints for</td>
<td>- DRC/ERC/ESD/ANT report</td>
</tr>
<tr>
<td>typical, worse and best corner case</td>
<td></td>
</tr>
<tr>
<td>- Full Datasheet/Application Note with</td>
<td></td>
</tr>
<tr>
<td>integration guidelines document</td>
<td></td>
</tr>
<tr>
<td>- Silicon characterization report when</td>
<td></td>
</tr>
<tr>
<td>available</td>
<td></td>
</tr>
</tbody>
</table>

Portfolio and Design Services:

V-Trans Microelectronics has been combining all the best practices and methodologies in analog and mixed-signal high speed interfaces design to answer the demanding market of high performance analog IPs using cheaper technologies such as 0.18um.

Our Portfolio covers a wide range of applications and can be customized on demand to answer exactly your specific needs.

Custom layout and back-end services are also available if you have a tied project schedule. Our experience includes high integration circuit such as network SOC, CPU and FPGA which allow us to provide a full solution for even more complex chip.

Please contact us to tell us how we could help you or for any analog IP information.

- High speed interfaces (LVDS serdes, Display Interfaces, DDRII, DDR3, PCI-X, HDMI rev1.1)
- Converters (video ADC 10b 170Mhz, Triple video DAC)
- Timing circuits (Audio PLL, Video PLL, DDR memory PLL, custom PLL)
- Low noise Crystal Oscillators
- Power management (LDO regulators, Power On Reset.)
- Video and WIMAX Analog Front end

V-TRANS Microelectronics – Shanghai Office
Tel: (+86)-021-54234123
v-trans@v-trans.com